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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HIEU P	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,460	NILSON, CHRIS	
	Examiner	Art Unit	
	Hieu Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16* is/are rejected.

7)☒ Claim(s) *15,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

On page 3 (¶ 9, on line 2), it appears that "a power control circuit " is repeated twice. Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence to all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "digital-to-analog converter" and a physical connection (**in series**) between second input from a second transistor and the first output of the first transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-4 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Aoki (US 6535065).

Regarding claims 1 and 3-4, Fig. 28 of Aoki discloses a power amplifier circuit comprising: a first transistor (see numeral 1) having a first input (gate) and a first output (collector); a second transistor (see numeral 41) having a second input (gate) and an emitter coupled in series with the first output of the first transistor; input circuit(s) (see numerals 3, 5, 8 and 9) coupled to the first input of the first transistor; and a power control circuit (see numerals 5, 6 and 95) coupled to the second input of the second transistor, the control circuit including; a time delay circuit that can be read from a combination of resistor and capacitor (see numeral 53 and 95); and a variable source (see variable current source from numeral 6).

Regarding claims 6 and 7, Aoki discloses everything claimed as applied to claim 1. In addition, Aoki discloses [col. 1, lines 19-24] the power amplifier circuit is included within a transmitter (transmission block) and [col. 1, lines 11-18] the amplifier circuit is included within a wireless data link transmitter (wireless communication system).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki in view of Matsunaga et al. (U.S 6759906).

Regarding claim 2, Aoki discloses everything claimed as applied to claim 1. In addition, Aoki discloses [col. 4, lines7-11] the control signal for the variable current source is fed from a control unit (not shown). Aoki lacks details structure or/and operation of the control unit. However Fig. 6 of Matsunaga discloses an analogous power amplifier wherein a variable source (see automatic power control circuit from numeral 74) includes a digital input from a logic (see Fig. 6, numeral 84) and a digital to analog converter (see numeral 85). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use digital control unit. The ordinary artisan would have been motivated to modify Aoki in the manner set forth above for at least the benefit of programmable control unit to compensate for changes in the amplifier optimal bias due to aging and temperature.

Regarding claim 9, Fig. 28 of Aoki discloses a power amplifier circuit comprising: a first transistor (see numeral 1) having a first input (gate) and a first output (collector); a second transistor (41) having a second input and its emitter coupled in series with the first output of the first transistor; an input circuit (not shown) coupled to the first input terminal of the first transistor; and a power control circuit coupled to the second input of the second transistor, the power control circuit including; an RC time delay circuit from a combination of resistor 53 and capacitor 95; and a variable current source (see numeral 6) including a control signal from a control unit (not shown) . Aoki doesn't

disclose specific details of the control unit. However Fig. 6 of Matsunaga discloses an analogous power amplifier wherein a variable source (see automatic power control circuit from numeral 74) includes a digital input from a logic (see Fig. 6, numeral 84) and a digital to analog converter (see numeral 85). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use digital control unit. The ordinary artisan would have been motivated to modify Aoki in the manner set forth above for at least the benefit of programmable control unit to compensate for changes in the amplifier optimal bias due to aging and temperature.

Regarding claim 10, Aoki discloses everything claimed as applied to claim 9 except for "one of the resistor and the capacitor are variable". However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use variable resistor of variable capacitor in Aoki's circuit. The ordinary artisan would have been motivated to modify Aoki in the manner set forth above for at least the purpose of adding flexibility to the power amplifier circuit.

Claim 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki.

Regarding claim 5, Aoki discloses everything claimed as applied to claim 4 except for "at least one of a resistor and capacitor are variable". However it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a variable resistor or/and capacitor. The ordinary artisan would have been motivated to modify Aoki in the manner set forth for at least the purpose of easiness in controlling the time delay.

Regarding claim 8, Aoki mentioned [Fig. 1, col. 1, lines 11-24] a prior art data link system comprising: a first receiver (reception block); and a first transmitter (transmission block) wherein each of a low-noise amplifier (103), an intermediate frequency amplifier (105) and a driver amplifier (111) and the like includes a variable-gain circuit. In addition, Fig. 28 of Aoki discloses a specific variable gain circuit including: a power control circuit coupled to a power control input, the power control circuit including: a time delay circuit that can be read from a combination of capacitor and resistor (see Fig. 28 numerals 95 and 53); and a variable current source (see numeral 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of "prior art" as mentioned in into Aoki's circuit by having a data link system comprising: a receiver, a transmitter and a power control circuit with a time delay circuit and a variable current source. The ordinary artisan would have been motivated to modify the prior art in the manner set forth above for at least the purpose of improving gain or amplification characteristic as mentioned by Aoki in col. 2, lines 16-14.

Claims 11,14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuura in view of Aoki.

Regarding claims 11, 14 and 16, Matsuura discloses [col. 10, lines 3-12] a method of controlling power output of an amplifier comprising:

Receiving a control signal from control means (see Fig. 2 of Matsuura, numeral 209); producing a stepped power control signal including a plurality of power control steps (note: a number of steps can be implicitly reflected from the executions of various signals and information as mentioned in col. 9, lines 55-64), wherein producing each

one of the plurality of steps includes: producing a step voltage; and applying the stepped power control signal to a power control input of the amplifier. Matsuura doesn't disclose the step of "applying a time delay to the step voltage". However Aoki discloses that the control signal (not shown) passes through a time delay before going to a power control input of the amplifier. It would have been obvious to one having ordinary skill in the art at the time the invention was made to "applying a time delay to the step voltage". The ordinary artisan would have been motivated to modify Matsuura in the manner set forth for at least the purpose of tuning the gain and frequency response.

Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuura and Aoki as applied to claim 11 above, and further in view of Matsunaga. Regarding claim 12, Matsuura and Aoki disclose everything claimed as applied to claim 11. Matsuura and Aoki fail to disclose the method wherein "the control signal is digital signal. However, Matsunaga discloses the method wherein the control signal from control logic (see Fig. 6, numeral 84) is a digital control signal that is input to a digital-to-analog converter to produce an analog control signal. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use digital control unit. The ordinary artisan would have been motivated to modify Aoki in the manner set forth above for at least the benefit of programmable control unit to compensate for changes in the amplifier optimal bias due to aging and temperature.

Allowable Subject Matter

Claim 15, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 15, the prior art of record fails to disclose or suggest a method of controlling power output of an amplifier " further comprising varying at least one aspect of the time delay to modify the time delay", in combination with the rest of the limitations of the claim(s).

Regarding claim 17, the prior art of record fails to disclose or suggest a method of controlling power output of an amplifier wherein "an elapsed time from a first one of the plurality of steps to a second one of the plurality of steps is less than a maximum ramp time", in combination with the rest of the limitations of the claim(s).

Regarding claim 18, the prior art of record fails to disclose or suggest a method of controlling power output of an amplifier wherein "a plurality of harmonics are substantially eliminated tat each one of the plurality of steps", in combination with the rest of the limitations of the claim(s).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number is 571-272-0218. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hieu Nguyen
AU: 2817

Zandra V. Smith
Primary Examiner

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